AF/2823

PATENT APPLICATION

PATENT AND TRADEMARK OFFICE

BEFORE THE HONORABLE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of

Hiroji AGA et al.

On Appeal from Group: 2823

Application No.: 09/857,803

Examiner: M. Estrada

Filed: June 11, 2001

Docket No.: 109725

For: METHOD FOR PRODUCING SOI WAFER AND SOI WAFER

APPEAL BRIEF TRANSMITTAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Attached hereto are three (3) copies of our Brief on Appeal in the above-identified application.

Also attached hereto is our Check No. 155098 in the amount of Three Hundred Thirty Dollars ($330.00) in payment of the Brief fee under 37 C.F.R. 1.17(c). In the event of any underpayment or overpayment, please debit or credit our Deposit Account No. 15-0461 as needed in order to effect proper filing of this Brief.

For the convenience of the Finance Division, two additional copies of this transmittal letter are attached.

Respectfully submitted,

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Date: June 16, 2004

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re the Application of:

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BRIEF ON APPEAL

06/17/2004 CNGUYEN 00000092 09857803
01 FC:1402 330.00 OP

Appeal from Group 2823

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I. INTRODUCTION

This is an appeal from an Office Action mailed January 16, 2004, finally rejecting claims 1-5 of the above-identified patent application. No claims are allowed.

A. Real Party in Interest

The real party in interest for this appeal and the present application is Shin-Etsu Handotai Co., Ltd., by way of an Assignment recorded in the U.S. Patent and Trademark Office at Reel 012012, Frame 0787.

B. Statement of Related Appeals and Interferences

There are presently no appeals or interferences, known to Appellants, Appellants' representative, or the Assignee, which will directly affect or be affected by or have a bearing upon the Board's decision in the pending appeal.

C. Status of Claims

Claims 1-3 and 6-8 are pending in this application. Claims 1-3 are finally rejected, and are on appeal. Claims 6-8 have been withdrawn from consideration as directed to a non-elected invention. Claims 4 and 5, and withdrawn claim 9, were canceled by Amendment on October 15, 2003. Claims 1-3 and 6-8 are set forth in the attached Appendix.

Claims 1 and 3 are independent. Claims 2, 6 and 7 depend, either directly or indirectly, from claim 1. Claim 8 depends from claim 3.

Appellants respectfully submit that the remarks below regarding each of claims 1-3 apply equally to their respective dependent claims 6-8. Thus, Appellants respectfully submit that, upon allowance of claims 1-3, claims 6-8 should be rejoined and allowed.

D. Status of Amendments

No Amendment After Final Rejection was filed. Appellants requested reconsideration in response to the Final Office Action mailed January 16, 2004. By an Advisory Action mailed May 10, 2004, it was indicated that the rejections were maintained.

II. THE INVENTION

A. Background of the Invention

Silicon on insulator (SOI) wafers and the methods for making them are of great importance for the semiconductor industry. Methods that can produce SOI wafers at low cost and with high quality are of particular importance for the commercial manufacture of semiconductor devices. The most desirable SOI wafers are those with good electronic and surface roughness characteristics.

One representative method of producing SOI wafers is the SMART CUT METHOD®. The SMART CUT METHOD® includes bonding a wafer implanted with hydrogen or other ions and then delaminating the wafer to produce an SOI wafer. See Specification, page 1, line 24 – page 2, line 3. This method is a technique for producing an SOI wafer, in which an oxide layer is formed on at least one of two silicon wafers, and hydrogen ions or rare gas ions are implanted into the top surface of one wafer to form a micro bubble –enclosed– layer. See Specification, page 2, lines 3-9. The ion-implanted surface of the wafer is then bonded to the other silicon wafer via the oxide layer, and the wafers are subjected to a delaminating heat treatment to delaminate one of the wafers as a thin film at the micro bubble layer as a cleavage plane. See Specification, page 2, lines 9-15. The other wafer is then subjected to a bonding heat treatment. See Specification, page 2, lines 15-17. By this process, it is possible to obtain an SOI wafer in which an SOI layer is firmly bonded on the silicon wafer. See Specification, page 1, line 24 – page 2, line 20.

However, after delamination at the micro bubble layer, the SOI layer surface has higher surface roughness when compared with a mirror-polished wafer used for usual device production. See Specification, page 2, lines 21-26. An SOI wafer having high surface roughness cannot be used for semiconductor device production without improving the surface roughness. See Specification, page 2, line 26 – page 3, line 1. Touch polishing is usually

performed to improve the surface roughness of the SOI wafer. See Specification, page 3, lines 1-4. Unfortunately, because the SOI layer is extremely thin, polishing may result in significant variations in SOI layer thickness due to the differing amounts of SOI layer removed as surface roughness is improved. See Specification, page 3, lines 5-9.

Thus, the semiconductor industry was presented with the problem of improving surface roughness after delamination without polishing the SOI wafer. One possibility for improving surface roughness of the SOI wafer was by performing a heat treatment of the SOI layer surface immediately after the delamination. See Specification, page 3, lines 10-13.

There are known methods for improving surface roughness by performing a heat treatment of the SOI layer surface immediately after the delamination. In one such process, a bonding heat treatment was performed in order to strengthen the bond between a support substrate and a single crystal silicon thin film. See Specification, page 3, lines 14-18. The bonding heat treatment was followed by another heat treatment, which was performed at a temperature in the range of 1000-1300°C for 10 minutes to 5 hours in a hydrogen atmosphere. See Specification, page 3, lines 18-22. Thus, it was known to reduce surface roughness by subjecting a hydrogen delaminated SOI wafer to hydrogen annealing. Hydrogen annealing, for tens of seconds to several tens of minutes, is generally performed in a batch processing type furnace. See Specification, page 4, line 8 – page 5, line 18.

Hydrogen annealing is only one method that may be used to improve surface roughness. In addition, any one of the known short-term annealing processes, such as rapid thermal annealing (RTA) or plasma annealing can be performed as a heat treatment for improving surface roughness. See Specification, page 5, lines 8-18. For example, RTA was considered a promising alternative for improving surface roughness, since RTA uses a rapid heating/rapid cooling apparatus and can be performed within an extremely short period of time. See Specification, page 5, lines 19-23. Because RTA could be performed quickly, it

was thought that the buried oxide layer would not be etched and, thus, COPs in the SOI layer could be eliminated. See Specification, page 5, lines 23-27. However, RTA is a single wafer process. See Specification, page 6, lines 18-23. From a manufacturing standpoint, short-term annealing processes, during which only a single wafer may be processed at any given time, are undesirable because they greatly increase manufacturing time and costs.

Although a batch processing furnace enables heat treatment of a large number of wafers over a long period of time, improving the surface roughness of SOI wafers by hydrogen annealing causes other detrimental effects on wafer quality. For example, if a single crystal silicon thin film SOI layer is formed from a wafer produced by the Czochralski (hereafter "CZ") method and has a small thickness of about 0.5 μm or less, hydrogen annealing causes a buried oxide layer to be etched by hydrogen gas that has penetrated through crystal originated particles (hereafter "COPs"), which are void-like grown-in defects. See Specification, page 4, lines 8-20. Other known atmospheres for heat treatments to improve surface roughness, such as argon, also cannot obviate the problem of etching through COPs. See Specification, page 4, lines 21-25. Thus, CZ wafers include COPs introduced therein during the crystal growth. See Specification, page 4, lines 25-27. If such a CZ wafer is used as a bond wafer to form an active layer (SOI layer), the COPs penetrate the SOI layer and form pinholes, which markedly degrade electric characteristics. See Specification, page 4, line 20 – page 5, line 7; page 6, line 24 – page 7, line 3. This is particularly problematic for extremely thin SOI layers, such as those employed in recently developed devices.

When a normal CZ wafer is used as the bond layer of the SOI wafer, pits of the buried oxide layer are formed by etching through COPs in the SOI layer during the hydrogen annealing treatment. See Specification, page 4, line 12 – page 5, line 7; page 6, line 24 – page 7, line 3. As disclosed in the instant specification and discussed above, Appellants

discovered, for the first time, that if an SOI wafer produced by using any one of an FZ wafer, an epitaxial wafer and a CZ wafer of which COPs at least on the surface are reduced is used as the bond wafer as described above, COPs in the SOI layer can be reduced or substantially completely eliminated. See Specification, page 18, line 26 – page 19, line 9. Etching of the buried oxide layer can be reduced or eliminated by the reduction and elimination of COPs from the SOI. See Specification, page 10, lines 3-8. Thus, the surface roughness of the SOI layer can be reduced by heat treatment under an atmosphere containing hydrogen or argon in a batch processing type furnace without producing pits of the buried oxide layer.

B. The Claimed Invention

The Appellants have developed, for the first time, methods for improving both the short period components and the long period components of surface roughness of an SOI layer surface, which has been delaminated by the hydrogen ion delamination method without polishing. For the first time, Appellants were able to secure uniformity of thickness of the SOI layer, as well as efficiently produce SOI wafers free from generation of pits due to COPs in SOI layers. In addition, Appellants were able to accomplish these results with increased throughput and efficiency. See Specification, page 7, lines 6-14.

When Appellants studied the improvement of the surface roughness of SOI wafers subjected to RTA, they discovered, for the first time, that only short period components of surface roughness were improved to a level comparable to that of the mirror-polished wafers usually used for device production. See Specification, page 6, lines 1-7; page 38, line 20 – page 40, line 26; Tables 1 and 2. The long period components of surface roughness were still very much inferior to those of the mirror-polished wafers. See Specification, page 6, lines 7-9; page 38, line 20 – page 40, line 26; Tables 1 and 2. Appellants further discovered that in order to improve the long period components of surface roughness by RTA, heat

treatment at high temperatures and for long periods of time was required. See Specification, page 6, lines 10-17; page 42, line 26 – page 43, line 12; Table 3.

Appellants decided to investigate alternative ways to improve both the short and long period components of SOI wafer surface roughness without etching the buried oxide layer or introducing COPs. The solutions Appellants chose to pursue were twofold. First, Appellants pursued methods of employing two consecutive heat treatments of the delaminated wafer under either hydrogen or inert atmosphere. See Specification, page 7, line 15 – page 9, line 16. Second, Appellants pursued methods of subjecting a wafer having a bonded portion delaminated from a Floating Zone (hereafter "FZ") wafer, an epitaxial wafer or a CZ wafer of which COPs at least on the surface are reduced, to a heat treatment under an atmosphere containing hydrogen or argon in a batch processing type furnace. See Specification, page 9, line 17 – page 11, line 18.

In particular, Appellants have unexpectedly found that an SOI wafer having improved surface roughness, uniform SOI layer thickness and being substantially free from COP-induced pits can be achieved by the method of independent claim 1. That is, Appellants found that an SOI wafer having improved surface roughness, uniform SOI layer thickness and being substantially free from COP-induced pits could be produced by the combination of:

- bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation;
- delaminating a wafer having an SOI layer at the micro bubble layer as a border, and
- subjecting the wafer having an SOI layer, in an atmosphere containing hydrogen or argon, to both a heat treatment utilizing a rapid heating/rapid cooling apparatus to improve the surface roughness of short periods of the SOI layer and a heat treatment utilizing a batch processing type furnace to improve the surface roughness of long periods of the SOI layer after the delamination step.

See Specification, page 7, lines 15-27; claim 1.

Appellants unexpectedly discovered that, if a wafer having an SOI layer is subjected to a heat treatment consisting of two stages utilizing separately a rapid heating/rapid cooling apparatus and a batch processing type furnace after the delamination as described above, surface crystallinity is restored and both the short period components and the long period components of surface roughness are improved. See Specification, page 8, line 27 – page 9, line 16; page 18, lines 13-25. Because this method does not use polishing such as touch polishing, thickness uniformity of the SOI layer is maintained. See Specification, page 8, lines 19-21.

The short period components of surface roughness are improved by the heat treatment by the rapid heating/rapid cooling apparatus, and the long period components of surface roughness are improved by heat treatment utilizing the batch processing type furnace. See Specification, page 8, lines 1-18; page 17, lines 21-27; page 38, line 20 – page 40, penultimate line; Tables 1 and 2. Large quantities of wafers can be subjected to heat treatments at the same time in the batch processing type furnace, resulting in higher throughput than other methods in which wafers are subjected to a heat treatment for a long period of time by the single wafer processing in a rapid heating/rapid cooling apparatus. See Specification, page 8, lines 11-18. Accordingly, the short period components of surface roughness are improved within an extremely short period of time by the heat treatment using an RTA apparatus, and in addition, a large number of wafers can be processed at one time when the long period components of surface roughness are improved in a batch processing type furnace.

Appellants have also unexpectedly found that an SOI wafer having improved surface roughness, uniform SOI layer thickness and being substantially free from COP-induced pits can be achieved by the method of independent claim 3. That is, Appellants found that an SOI

wafer having improved surface roughness, uniform SOI layer thickness and being substantially free from COP-induced pits could be produced by the combination of:

- bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation, wherein an FZ wafer, an epitaxial wafer or a CZ wafer of which COPs at least on a surface are reduced, is used as the bond wafer;
- delaminating a wafer having an SOI layer at the micro bubble layer as a border,
- subjecting the wafer having an SOI layer to a heat treatment under an atmosphere containing hydrogen or argon in a batch processing type furnace after the delamination step.

See Specification, page 9, line 17 – page 10, line 2; claim 3.

Appellants discovered for the first time that if an SOI wafer is produced by using as the bond wafer any one of an FZ wafer, an epitaxial wafer and a CZ wafer of which COPs at least on the surface are reduced as described above, COPs in the SOI layer can be reduced or substantially completely eliminated. See Specification, page 10, lines 3-8; page 18, line 26 – page 19, line 9. Reduction and elimination of COPs from the SOI layer reduces or eliminates etching of the buried oxide layer during heat treatments at high temperatures for long periods of time in a batch processing type furnace. See Specification, page 10, lines 8-12. Thus, the surface roughness of the SOI layer can be reduced by heat treatment under an atmosphere containing hydrogen or argon in a batch processing type furnace without producing pits in the buried oxide layer.

Specifically, and as disclosed in the specification, SOI wafers are produced by using as a bond wafer a CZ wafer produced from a single crystal ingot of which grown-in defects, such as COPs, are reduced for the whole crystal by controlling V/G (V: pulling rate, G: temperature gradient along the direction of solid-liquid interface of crystal) (see, for example, Example 3), or an epitaxial wafer (see, for example, Example 4), respectively, and then are

subjected to a heat treatment utilizing a batch processing type furnace. See Specification, page 40, line 27 – page 43, line 12; Table 3. Consequently, the surface roughness for both 1 μm square (short period components) and 10 μm square (long period components) are improved up to the same level as Examples 1 and 2 corresponding to claims 1 and 2. See Specification, Table 2. By producing an SOI wafer by using the wafer recited in claim 3 as a bond wafer, and after the delamination, performing a heat treatment in the atmosphere containing hydrogen or argon, generation of pits due to COPs can be prevented and both short and long period components of surface roughness can be sufficiently improved.

III. THE APPLIED REFERENCES

The applied references are:

Japanese Patent Application Publication No. JP 10-275905 to Yamamoto (hereafter, "Yamamoto");

U.S. Patent Application Publication No. US 2002/0127820 to Sato (hereafter, "Sato");

U.S. Patent No. 6,074,479 to Adachi et al. (hereafter, "Adachi"); and

Stanley Wolf & Richard N. Tauber SILICON PROCESSING FOR THE VLSI ERA: Volume 1: Process Technology 23-25 (Lattice Press 1986) (hereafter, "Wolf").

IV. ISSUES

The issues on appeal are:

1) whether claims 1 and 2 would have been obvious under 35 U.S.C. §103(a) over the combination of Yamamoto and Sato; and

2) whether claim 3 would have been obvious under 35 U.S.C. §103(a) over the combination of Yamamoto and Sato and further in view of Adachi and Wolf.

V. GROUPING OF CLAIMS

Each claim of this patent application is separately patentable, and upon issuance of a patent will be entitled to a separate presumption of validity under 35 U.S.C. §282. For

convenience in handling of this appeal, the rejected claims will be grouped and argued as follows:

Group I – claims 1 and 2; and

Group II – claim 3.

Thus, pursuant to 37 C.F.R. §1.192(c)(7), in this Appeal, the rejected claims within each Group will stand or fall together.

VI. ARGUMENT

The Examiner rejects claims 1 and 2 under 35 U.S.C. §103(a) over the combination of Yamamoto and Sato. The Examiner rejects claim 3 under 35 U.S.C. §103(a) over the combination of Yamamoto and Sato as applied to claims 1 and 2, and further in view of Adachi and Wolf.

In these rejections, the Examiner has consistently improperly applied the law relating to obviousness, and has failed to establish even a prima facie case of obviousness. Proper application of the law and consideration of the cited references demonstrates that no prima facie case of obviousness has been shown.

A. Factual Inquiries to Determine Obviousness/NonObviousness

Several basic factual inquiries must be made in order to determine obviousness or non-obviousness of the claims of a patent application under 35 U.S.C. §103(a). These factual inquiries are set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966):

> Under §103, the scope and content of the prior art are to be determined; difference between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or non-obviousness of the subject matter is determined.

383 U.S. at 17-18, 148 USPQ 467. This involves considering the scope and content of the prior art, the differences between the prior art and the claims at issue, the level of ordinary

skill in the art, and any secondary considerations that may be present. 383 U.S. at 17, 148 USPQ at 467.

In addition, the combination of references to support a rejection requires a motivation or suggestion in the art that one should carry out the claimed invention, and would have a reasonable expectation of success in doing so. In re Vaeck, 947 F.2d 488, 493, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991). In the present case, proper consideration of the actual teachings of the cited references and the level of ordinary skill in the art provide no motivation or suggestion that the cited references, in particular Yamamoto and Sato, should or could be combined.

Evidence of secondary considerations such as unexpected results, including such evidence in the specification, must be taken into account. MPEP §2144.08 II.A.

B. Claims 1 and 2 Are Patentable Over the Cited References

Claim 1 sets forth a "method for producing an SOI wafer by the hydrogen ion delamination method comprising at least a step of bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation and a step of delaminating a wafer having an SOI layer at the micro bubble layer as a border, wherein, after the delamination step, the wafer having an SOI layer is subjected, in an atmosphere containing hydrogen or argon, to both a heat treatment utilizing a rapid heating/rapid cooling apparatus to improve the surface roughness of short periods of the SOI layer and a heat treatment utilizing a batch processing type furnace to improve the surface roughness of long periods of the SOI layer." Claim 2 depends from claim 1 and incorporates all the limitations of claim 1. As discussed in detail below, neither of the cited references, alone or in combination, teach or suggest the method of claim 1 or the beneficial results that proceed from this combination.

1. Yamamoto Does Not Teach or Suggest the Claimed Invention

Yamamoto is cited as disclosing a method for producing an SOI wafer by the hydrogen delamination method. See January 16, 2004 Office Action, page 2, lines 12-17. The method disclosed by Yamamoto includes steps of bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation and delaminating the wafer. See Yamamoto, [0008]-[0009]; Fig. 1. After the delamination step, Yamamoto discloses subjecting the wafer to RTA under hydrogen atmosphere to improve the surface roughness of the SOI layer. See Yamamoto, [0010]; Fig. 1.

However, claim 1 clearly includes the limitation that the wafer having an SOI layer be subjected to both a heat treatment utilizing a rapid heating/rapid cooling apparatus to improve the short period components of surface roughness of the SOI layer and a heat treatment utilizing a batch processing type furnace to improve the long period components of surface roughness for the SOI layer. This requirement reflects Appellants' discovery that RTA, such as the heat treatment in Yamamoto, improves only the short period components of surface roughness to a level comparable to that of mirror-polished wafers. See Specification, page 6, lines 1-7; page 17, lines 21-27; page 38, line 20 – page 40, penultimate line; Tables 1 and 2. After the process of Yamamoto is performed, the long period components of surface roughness are still inferior to mirror-polished wafers after RTA treatments. See Specification, page 6, lines 7-9; page 38, line 20 – page 40, penultimate line; Tables 1 and 2. Appellants discovered, for the first time, that in order to improve the long period components of surface roughness, a heat treatment using high heat for a long period of time is required. See Specification, page 6, lines 10-17; page 42, penultimate line – page 43, line 12; Table 3.

Yamamoto performs a heat treatment in hydrogen atmosphere, but does not teach or suggest utilizing both a rapid heating/rapid cooling apparatus and a batch processing type

furnace to improve both short period components and long period components of surface roughness of the SOI layer.

Thus, Yamamoto alone does not disclose, teach or suggest the invention of claims 1 and 2.

2. Sato Does Not Teach or Suggest the Claimed Invention

Sato is cited for its teachings of a semiconductor substrate, on which an insulating layer is formed and hydrogen ions are implanted, joining the semiconductor substrate to a support substrate and delaminating the resulting structure. See January 16, 2004 Office Action, page 2, lines 20-23. Sato is further cited as disclosing that after delamination, the structure is subjected to a heat treatment in a hydrogen annealing furnace. See January 16, 2004 Office Action, page 2, lines 23-25.

Sato discloses the production of SOI wafers and that wafers having an SOI structure are set in a vertical-type hydrogen annealing furnace and subjected to a heat treatment in a hydrogen atmosphere for one to four hours at 1100°C. See Sato, [0207], [0273]. Although Sato performs a heat treatment in hydrogen atmosphere, Sato, like Yamamoto, does not teach or suggest utilizing both a rapid heating/rapid cooling apparatus and a batch processing type furnace to improve both short periods and long periods of surface roughness of the SOI layer. Thus, the Sato method improves the long period components of surface roughness. The short period components of surface roughness, however, are not improved by the Sato process.

In addition, the Sato method does not produce an SOI wafer by the hydrogen ion delamination method, as described in claim 1. While the Office Action asserts that Sato discloses implanting hydrogen ions into a semiconductor surface, Sato itself makes clear that a substrate having a porous silicon layer is prepared by the anodization method using hydrofluoric acid, for example, and a nonporous microcrystalline layer is grown on the porous silicon layer, in which hydrogen ions are not implanted into the substrate. Sato's method is

not a hydrogen ion delamination method, such as that described in claim 1. See Sato, [0135]-[0138], [0157]-[0158], Fig. 10A-10E; claims 1 and 2.

Thus, Sato alone does not disclose, teach or suggest the invention of claims 1 and 2.

3. Yamamoto and Sato Are Improperly Combined

Furthermore, Yamamoto and Sato are improperly combined, as there is no motivation for their combination.

Two references cannot be combined to render obvious a claimed invention where there is no motivation in the references or elsewhere to make the asserted combination. For example, the Federal Circuit held in In re Oetiker that "[t]here must be some reason, suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination." 977 F.2d 1443, 1447, 24 USPQ2d 1443, 1446 (Fed. Cir. 1992). See also In re Geiger, 815 F.2d 686, 688, 2 USPQ2d 1276, 1278 (Fed. Cir. 1987) ("Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination."). That is, it is not enough that a combination of references may be capable of being combined and modified to arrive at a claimed invention. To the contrary, the prior art must have suggested the desirability of such modification to one of ordinary skill in the art at the time the invention was made.

In the present case, the Office Action asserts that the combination of Yamamoto and Sato teaches annealing by either a furnace or RTA and that, for this reason, it would have been within the scope of one of ordinary skill in the art to use RTA and furnace heating. See January 16, 2004 Office Action, page 2, line 25 – page 3, line 10. However, there is no motivation to combine Yamamoto and Sato in the manner asserted by the Examiner.

Appellants respectfully submit that the Office Action is selectively combining only the heat treatment processes of Yamamoto and Sato, without any motivation to do so. One of

ordinary skill in the art would have understood that the surface roughness of the SOI layer could be improved by either hydrogen annealing using an RTA or hydrogen annealing using a batch-type furnace. However, without the knowledge or further investigation to discover that the short period components of surface roughness are improved by a rapid heating/rapid cooling apparatus and the long period components of surface roughness of the SOI layer are improved by a batch processing type furnace, one of ordinary skill in the art would not have been motivated to selectively combine the heat treatments of Yamamoto and Sato. That is, because surface roughness generally can be improved by either RTA or batch type furnaces, one of ordinary skill in the art would not have been motivated to perform two successive heat treatments in which two apparatuses of different types are required without a compelling reason to do so, at least because performing two heat treatments adds to the cost and time needed to perform a function apparently performed by one heat treatment.

Prior to Appellants' discoveries, it was unknown in the art that only the short period components of surface roughness are improved by rapid heating/rapid cooling apparatus and only the long period components of surface roughness are improved by batch type furnaces. In particular, it was not known that neither type of heat treatment improves both the surface roughness of short and long period components. None of the cited references disclose or suggest such a possibility. The art of record points to the need for only one heat treatment to improve surface roughness and does not contemplate the use of more than one heat treatment, or the use of more than one type of heat treatment. Thus, without a compelling reason, such as the knowledge provided by Appellants that short period components of surface roughness are improved by rapid heating/rapid cooling apparatus and long period components of surface roughness are improved by batch type furnaces, such a two-stage process would not have been performed.

The Office Action asserts that in view of the individual teachings of the cited references, it would have been obvious to one of ordinary skill in the art to combine the teachings of Yamamoto with Sato to derive a two-stage heat treatment process as set forth in claim 1. See January 16, 2004 Office Action, page 2, line 25 – page 3, line 10. However, the Office Action has failed to provide any evidence to support that one of ordinary skill in the art would have been motivated to combine the teachings of the cited references as asserted.

Neither reference teaches or suggests that it would be desirable or advantageous to subject an SOI wafer to an additional heat treatment step, which would have required additional time and cost for no apparent reason. Although both references teach a heat treatment to planarize a laminated surface, each reference only teaches or suggests a one-stage heat treatment. Neither reference teaches or suggests that an additional or subsequent heat treatment in the complementary apparatus would be desirable or advantageous.

In fact, each of Yamamoto and Sato appear to be directed to alternative methods for carrying out the same heat treatment process. Neither reference teaches or suggests that its disclosed process is deficient in any way, such that the disclosed process should be supplemented by a second heat treatment process. One of ordinary skill in the art, looking at the disclosures of Yamamoto and Sato, would not have been motivated to combine their separate teachings into a single, two-step process. Instead, one of ordinary skill in the art would only have been motivated to use either the process of Yamamoto or the process of Sato, since both are disclosed to be suitable and effective for their intended purpose.

Clearly, the only motivation for combining the cited references comes from a hindsight reconstruction of the claimed invention. The Office Action has based the rejection solely on picking and choosing the instant claim limitations from two cited references.

It has clearly been held that the reason, suggestion or motivation for combining the references "can not come from the applicant's invention itself." In re Oetiker, 977 F.2d at 1447,

24 USPQ2d at 1446. That is, the motivation for combining the references can not be a product of hindsight reconstruction of the claimed invention based on Appellants' own disclosure. Such a hindsight reconstruction has clearly been made in the January 16, 2004 Office Action.

The Office Action asserts that the claimed invention would have been obvious based on a hindsight selection of the claimed limitations, as evidenced by the teachings of the cited references, neither of which would suggest to one skilled in the art that the teachings could or should be combined and then further modified to provide the claimed invention. Such a combination is improper because the references, viewed by themselves and not in retrospect, must suggest the combination asserted by the Office Action. In re Shaffer, 229 F.2d 476, 108 USPQ 326 (C.C.P.A. 1956); In re Stoll, 523 F.2d 1392, 187 USPQ 481 (C.C.P.A. 1975).

As discussed above, the references do not provide any motivation for combining the separately disclosed heat treatment processes. Sato discloses hydrogen annealing to improve surface roughness. Yamamoto discloses that surface roughness may be improved by heat treatment using either RTA or a batch processing type furnace. Each reference teaches a single heat treatment. Neither reference teaches or suggests that an additional or subsequent heat treatment in the complementary apparatus would be desirable or advantageous.

In addition, it is impermissible within the framework of 35 U.S.C. §103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation that the reference fairly suggests to one of ordinary skill in the art. In re Wesslau, 147 USPQ 391, 393 (CCPA 1965). The Office Action apparently takes the position that the teaching of different types of heat treatments for the same purpose, without additional motivation, is sufficient to support combining Yamamoto and Sato to arrive at the two-stage heat treatment of claim 1. However, both references teach only the use of one heat treatment; neither reference suggests a two-stage treatment. The Office

Action thus is impermissibly picking and choosing claim limitations from the references, without consideration of the teachings of the references as a whole.

Furthermore, neither reference teaches or suggests that the surface roughness of both long and short periods may be improved by subjecting the SOI wafers to a two-stage heat treatment process. As stated in the specification, at page 8, lines 5-11, "surface crystallinity is restored and the surface roughness of short periods is improved in the heat treatment by the rapid heating/rapid cooling apparatus, and the surface roughness of long periods can be improved by the heat treatment utilizing the batch processing type furnace." Thus, the treatment of the SOI wafers under different conditions in two different apparatus yields results that would not be attainable using the methods described in the cited references because the references only teach the use of individual, alternative heat treatment processes.

Further, Yamamoto and Sato are not properly combinable because the Sato method differs completely from the method of Yamamoto. A skilled artisan would not look to the teachings of Sato, which relate to producing an SOI wafer by growing a non-porous silicon layer on a porous silicon layer that has been prepared by anodization (see Sato, [0135]-[0138], [0157]-[0158], Figs. 10A-10E; claims 1, 2), to modify the invention of Yamamoto, which relates to producing an SOI wafer by hydrogen ion delamination (see Yamamoto, Abstract), or vice versa.

The only motivation for combining the cited references in the manner asserted in the Office Action derives from the disclosure of the present application, which is clearly improper. Accordingly, one of ordinary skill in the art would not have been motivated to perform a two-stage heat treatment by utilizing two different types of heat treatment apparatus, as set forth in claim 1.

4. Yamamoto and Sato Fail to Suggest the Unexpected Results Achieved by the Claimed Invention

Further, the method of claim 1 produces unexpected results.

As shown in Tables 1 and 2 of Appellants' specification, treating a silicon wafer with an RTA apparatus improves the short period components of surface roughness. Examples 1 and 2 and Comparative Example 3 all show markedly improved short period components of surface roughness, with each decreasing from 7.21 nm, 7.50 nm and 7.45 nm, respectively, to 0.18 nm, 0.20 nm and 0.21 nm after heat treatment. See Specification, page 38, line 20 – page 40, line 26; Tables 1 and 2. However, the long period components of surface roughness of Comparative Example 1, which was only subjected to an RTA heat treatment, were reduced only from 5.75 nm to 1.60 nm, while the long period components of surface roughness of Examples 1 and 2, which were subjected to both a two stage heat treatment as set forth in claim 1, were reduced from 5.50 nm and 5.80 nm to 0.28 nm and 0.30 nm respectively. See Specification, page 38, line 20 – page 40, line 26; Tables 1 and 2. Prior to Appellants' discoveries, it was unknown in the art that only the short period components of surface roughness are improved by rapid heating/rapid cooling apparatus. In particular, it was not known that neither RTA nor batch type processing heat treatments improve both the short and long period components of surface roughness. See Specification, page 9, lines 1-7; page 18, lines 13-25.

Neither of the cited references, nor their combination, disclose or suggest the unexpected results achieved by the method of claim 1, and the Office Action has failed to provide any evidence to support that one of ordinary skill in the art would have understood that only short period components of surface roughness are improved by the heat treatment by the rapid heating/rapid cooling apparatus, or that only long period components of surface roughness are improved by heat treatment utilizing the batch processing type furnace, prior to

Appellants' invention. This knowledge was disclosed for the first time in the present application.

The art of record points to the need for only one heat treatment to improve surface roughness and does not contemplate the use of more than one heat treatment, or the use of more than one type of heat treatment. Thus, without a compelling reason, such as the knowledge provided by Appellants that short period components of surface roughness are improved by rapid heating/rapid cooling apparatus and long period components of surface roughness are improved by batch type furnaces, such a two-stage process would not have been performed.

5. Conclusion

For at least these reasons, Yamamoto and Sato, alone or in combination, do not teach or suggest the invention of claims 1 and 2. Accordingly, reconsideration and withdrawal of this rejection are requested.

C. Claim 3 Is Patentable Over the Cited References

Claim 3 sets forth a "method for producing an SOI wafer by the hydrogen ion delamination method comprising at least a step of bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation and a step of delaminating a wafer having an SOI layer at the micro bubble layer as a border, wherein an FZ wafer, an epitaxial wafer or a CZ wafer of which COPs at least on surface are reduced is used as the bond wafer, and the wafer having an SOI layer is subjected to a heat treatment under an atmosphere containing hydrogen or argon in a batch processing type furnace after the delamination step." As discussed in detail below, none of the cited references, alone or in combination, teach or suggest the method of claim 3 or the beneficial results that proceed from this combination.

The Office Action applies Yamamoto and Sato to claim 3 in the same way the references were applied to claims 1 and 2, discussed in detail above. However, Yamamoto and Sato, alone or in combination, do not disclose, teach or suggest the invention of claim 3.

1. Yamamoto Does Not Teach or Suggest the Claimed Invention

Yamamoto discloses subjecting an SOI wafer that has been delaminated to RTA under hydrogen atmosphere to improve the surface roughness of the SOI layer. See Yamamoto, [0008]-[0010]; Fig. 1.

However, claim 3 clearly includes the limitation that the wafer having an SOI layer, in which an FZ wafer, an epitaxial wafer or a CZ wafer having reduced COPs at least on the surface is used as the bond wafer, be subjected to a heat treatment utilizing a batch processing type furnace, to improve the long period components of surface roughness for the SOI layer. This requirement reflects Appellants' discovery that in order to improve the long period components of surface roughness, a heat treatment using high heat for a long period of time is required. See Specification, page 6, lines 10-17; page 42, penultimate line – page 43, line 12; Table 3.

Yamamoto performs a heat treatment in hydrogen atmosphere, but does not teach or suggest utilizing a batch processing type furnace to improve the long period components of surface roughness of the SOI layer.

Thus, Yamamoto alone does not disclose, teach or suggest the invention of claim 3.

2. Sato Does Not Teach or Suggest the Claimed Invention

Sato discloses the production of SOI wafers and that wafers having an SOI structure are set in a vertical-type hydrogen annealing furnace and subjected to a heat treatment in a hydrogen atmosphere for one to four hours at 1100°C. See Sato, paragraphs [0207], [0273].

However, claim 3 clearly includes the limitation that the wafer having an SOI layer, in which an FZ wafer, an epitaxial wafer or a CZ wafer having reduced COPs at least on the

surface is used as the bond wafer, be subjected to a heat treatment utilizing a batch processing type furnace, to improve the long period components of surface roughness for the SOI layer. This requirement reflects Appellants' discoveries that in order to improve the long period components of surface roughness, a heat treatment using high heat for a long period of time is required and that if a wafer without COPs or whose COPs are reduced is used as a bond wafer, the COPs in SOI layer can be reduced or substantially eliminated and a heat treatment at a high temperature for a long period of time in a batch processing type furnace, without etching of the buried oxide layer due to COPs is not caused, becomes possible. See Specification, page 6, lines 10-17; page 9, lines 8-16; page 10, lines 3-12; page 11, lines 12-18; page 42, penultimate line – page 43, line 12; Table 3. That is, it is possible to perform heat treatments in batch processing type furnaces without etching the buried oxide layer. Thus, by using a CZ wafer in which the grown-in defects, such as COPs, are reduced, an SOI wafer having good surface roughness in both long and short periods can be obtained.

Specifically, and as disclosed in the specification, SOI wafers are produced by using as a bond wafer a CZ wafer produced from a single crystal ingot of which grown-in defects, such as COPs, are reduced for the whole crystal by controlling V/G (V: pulling rate, G: temperature gradient along the direction of solid-liquid interface of crystal) (see, for example, Example 3), or an epitaxial wafer (see, for example, Example 4), respectively, and then are subjected to a heat treatment utilizing a batch processing type furnace. See Specification, page 40, line 27 – page 43, line 12; Table 3. Consequently, the surface roughness for both 1 μm square (short period components) and 10 μm square (long period components) are improved up to the same level as Examples 1 and 2 corresponding to claims 1 and 2. See Specification, Table 2. By producing an SOI wafer by using the wafer recited in claim 3 as a bond wafer, and after the delamination, performing a heat treatment in the atmosphere

containing hydrogen or argon, generation of pits due to COPs can be prevented and both short and long period components of surface roughness can be sufficiently improved.

Although Sato performs a heat treatment in hydrogen atmosphere, Sato, like Yamamoto, does not teach or suggest that by producing an SOI wafer by using the wafer recited in claim 3 as a bond wafer, and after the delamination, performing a heat treatment in the atmosphere containing hydrogen or argon, generation of pits due to COPs can be prevented and both short and long period components of surface roughness can be sufficiently improved.

In addition, the Sato method does not produce an SOI wafer by the hydrogen ion delamination method, as described in claim 3. While the Office Action asserts that Sato discloses implanting hydrogen ions into a semiconductor surface, Sato itself makes clear that a substrate having a porous silicon layer is prepared by the anodization method using hydrofluoric acid, for example, and a nonporous microcrystalline layer is grown on the porous silicon layer, in which hydrogen ions are not implanted into the substrate. Sato's method is not a hydrogen ion delamination method, such as that described in claim 1. See Sato, paragraphs [0135]-[0138], [0157]-[0158], Fig. 10A-10E; claims 1 and 2.

Thus, Sato alone does not disclose, teach or suggest the invention of claim 3.

3. All Four Cited References Fail to Suggest the Claimed Invention

As admitted by the Office Action, neither Yamamoto nor Sato disclose or suggest that a CZ wafer having reduced COPs may be used as the bond wafer or that such a CZ wafer may be produced from a single ingot. See January 16, 2004 Office Action, page 3, lines 15-17.

The Office Action suggests that it would have been within the scope of one of ordinary skill in the art to use the Adachi CZ wafer as the bond wafer and thus enhance the quality of the finished product. See January 16, 2004 Office Action, page 3, lines 19-22. Appellants respectfully disagree with the Office Action's conclusions. Contrary to the

assertion of the Office Action, one of ordinary skill in the art would not have been motivated to combine the teachings of Adachi with those of Yamamoto and Sato.

Wolf generally teaches the subjects of silicon single crystal growth and wafer preparation. Wolf teaches wafer preparation from silicon single crystals grown by both the CZ and FZ methods. Wolf is cited only for its disclosure of general wafer preparation from CZ silicon single crystals. See January 16, 2004 Office Action, page 4, lines 1-2.

Adachi was cited as disclosing a CZ silicon single crystal bond wafer, in which the COPs on at least the surface have been reduced. See January 16, 2004 Office Action, page 3, lines 18-19. Adachi discloses that wafers stacked up as shown in Fig. 1b are annealed in a furnace so that grown-in defects, which give rise to surface COP and internal COP, are eliminated. See Adachi, col. 1, lines 25-33.

However, none of the cited references teaches or suggests that a CZ wafer in which COPs on the surface are reduced should be used as a bond wafer because none of the references recognize that a buried oxide layer is etched through COPs by hydrogen gas. Thus, one of ordinary skill in the art would not have been motivated to combine the teachings of Adachi with the cited primary references.

In contrast to claim 3, none of the cited references disclose, teach or suggest that the buried oxide layer is etched through COPs in the SOI layer when the SOI wafer after the delamination is subjected to heat treatment in the atmosphere containing hydrogen or argon. Likewise, none of the cited references teach or suggest a solution to this problem, or any motivation to combine these references to solve the unspecified problem.

None of the references disclose, teach or suggest that generation of pits can be prevented, and none of the references disclose, teach or suggest that both short and long periods of surface roughness can be sufficiently improved by employing a bond wafer whose COPs in an SOI layer are reduced, and performing a heat treatment in the atmosphere

containing hydrogen or argon. Thus, there is no motivation or suggestion in the cited references to use an Adachi CZ wafer as the bond wafer. One of ordinary skill in the art would not have been motivated to combine or modify these references to derive the subject matter of claim 3, and the cited references, alone or in combination, do not disclose, teach or suggest the subject matter of claim 3.

Because the rejection relies on the combination of Yamamoto and Sato as the primary references, Appellants respectfully submit that the rejection should be withdrawn. Even if one of ordinary skill in the art were to combine the teachings of Adachi and Wolf with those of Yamamoto and Sato, the citation of Adachi and Wolf fails to cure the deficiencies identified in the teachings of Yamamoto and Sato for the reasons discussed above.

4. Conclusion

Thus, Yamamoto, Sato, Adachi and Wolf, alone or in combination, would not have rendered claim 3 obvious. Accordingly, reconsideration and withdrawal of this rejection is requested.

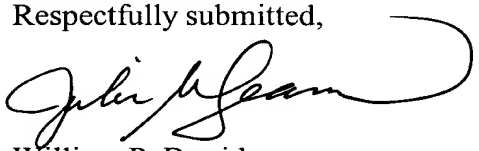
D. Conclusion

Considered in light of all of the factors relevant to an obviousness determination, Yamamoto, Sato, Adachi and Wolf, alone and together, do not teach or suggest the claimed combination or the unexpected results achieved thereby. Accordingly, reconsideration and withdrawal of the rejections are respectfully requested.

VII. CONCLUSION

For all of the reasons discussed above, it is respectfully submitted that claims 1-3 and 6-8 define patentable subject matter under 35 U.S.C. §103(a) over the cited references, and are thus in condition for allowance. For all of the above reasons, Appellants respectfully request this Honorable Board to reverse the rejections of claims 1-3.

Respectfully submitted,



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APPENDIX A

CLAIMS:

1. (Previously Presented) A method for producing an SOI wafer by the hydrogen ion delamination method comprising at least a step of bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation and a step of delaminating a wafer having an SOI layer at the micro bubble layer as a border, wherein, after the delamination step, the wafer having an SOI layer is subjected, in an atmosphere containing hydrogen or argon, to both a heat treatment utilizing a rapid heating/rapid cooling apparatus to improve the surface roughness of short periods of the SOI layer and a heat treatment utilizing a batch processing type furnace to improve the surface roughness of long periods of the SOI layer.

2. (Original) The method for producing an SOI wafer according to Claim 1, wherein the two-stage heat treatment is performed by subjecting the wafers to a heat treatment in the rapid heating/rapid cooling apparatus and then a heat treatment in the batch processing type furnace.

3. (Original) A method for producing an SOI wafer by the hydrogen ion delamination method comprising at least a step of bonding a base wafer and a bond wafer having a micro bubble layer formed by gas ion implantation and a step of delaminating a wafer having an SOI layer at the micro bubble layer as a border, wherein an FZ wafer, an epitaxial wafer or a CZ wafer of which COPs at least on surface are reduced is used as the bond wafer, and the wafer having an SOI layer is subjected to a heat treatment under an atmosphere containing hydrogen or argon in a batch processing type furnace after the delamination step.

4. (Canceled)

5. (Canceled)

6. (Withdrawn) An SOI wafer produced by the method according to Claim 1, which has an RMS value of 0.5 nm or less concerning surface roughness for both of 1 μm square and 10 μm square.

7. (Withdrawn) An SOI wafer produced by the method according to Claim 2, which has an RMS value of 0.5 nm or less concerning surface roughness for both of 1 μm square and 10 μm square.

8. (Withdrawn) An SOI wafer produced by the method according to Claim 3, which has an RMS value of 0.5 nm or less concerning surface roughness for both of 1 μm square and 10 μm square.

9. (Canceled)